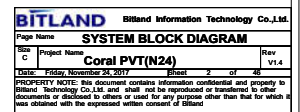
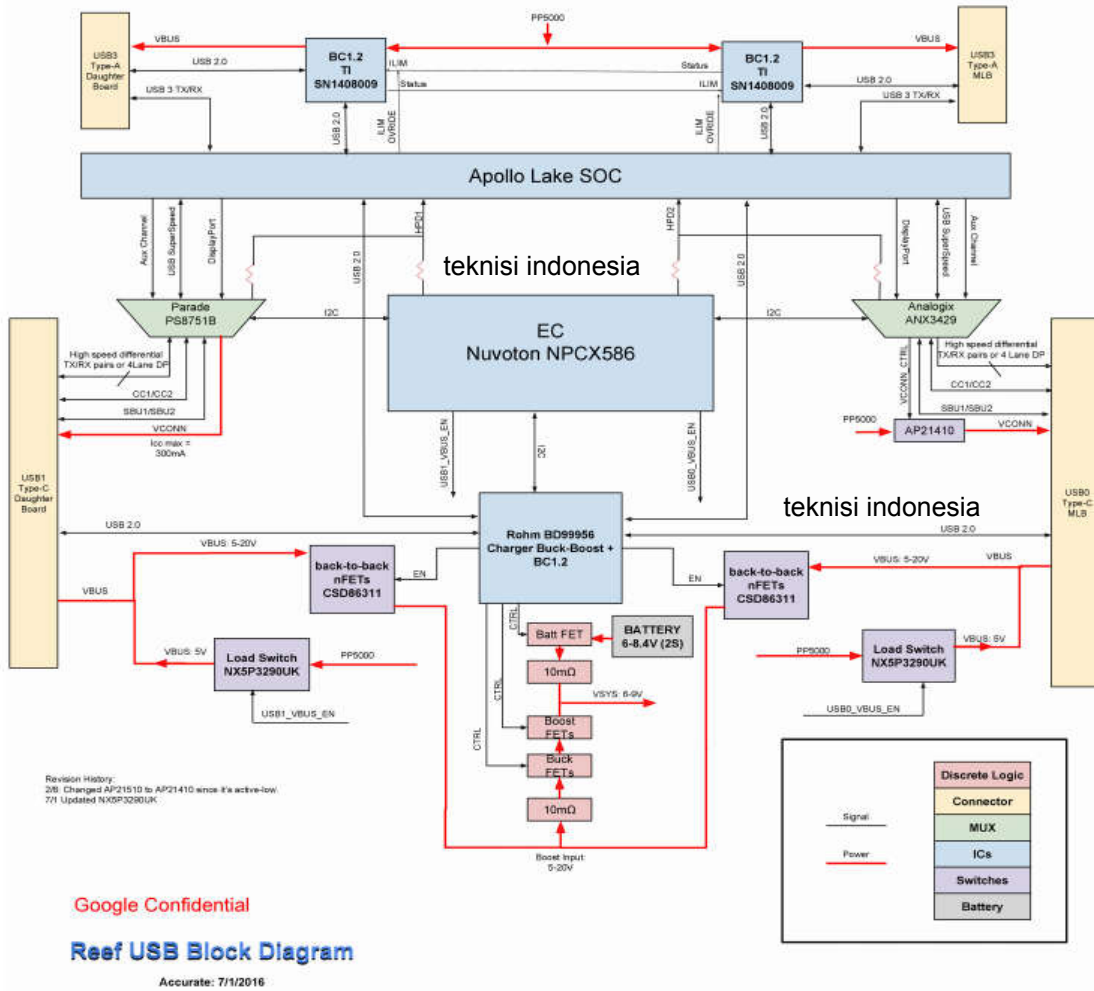


[illegible]





BITLAND			
USB TYPE-C BLOCK DIAGRAM			
Doc	Project Name	Rev	Rev
C	Coral PVT(N24)	1	V1.4
Date	Friday, November 24, 2017	Page	3 of 4
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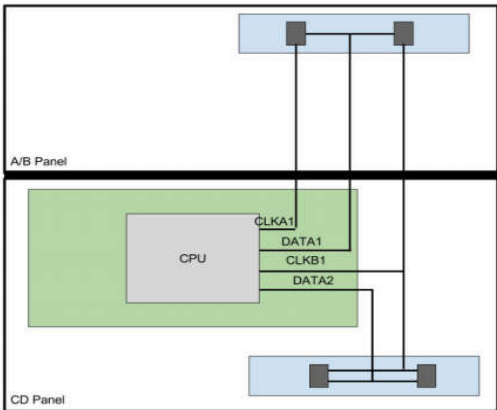
EC I2C Address

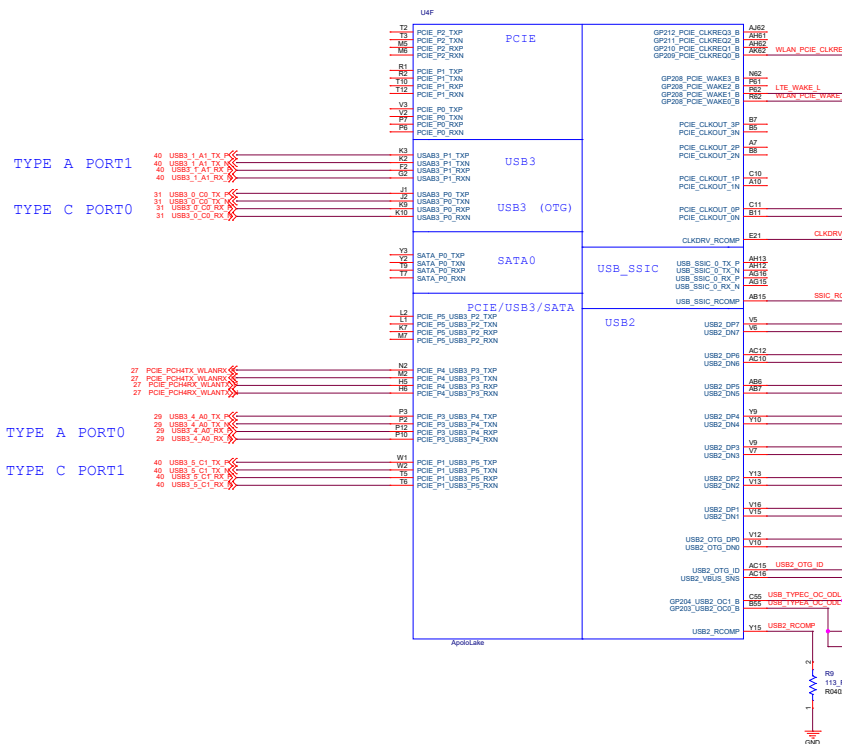
Bus	Alternate function	Schematic net name	Device1	Address1 (7bit)	Device2	Address2
I2C0_0	-	EC_I2C_USB_C0_PD	Analogix TCPC	0x50 (check 7/8 bit)		
I2C0_1	-	EC_I2C_USB_C1_PD	Parade TCPC	0x0B		
I2C1	-	EC_I2C_GYRO	BOSCH Gyro	0x68		
I2C2	-	EC_I2C_SENSOR	Kionix Accelerometer	0x1F	Bosch Barometer (removed)	0x76
I2C3	-	EC_I2C_POWER	Rohm Charger	0x09	Battery Pack	TBD

AP I2C Address

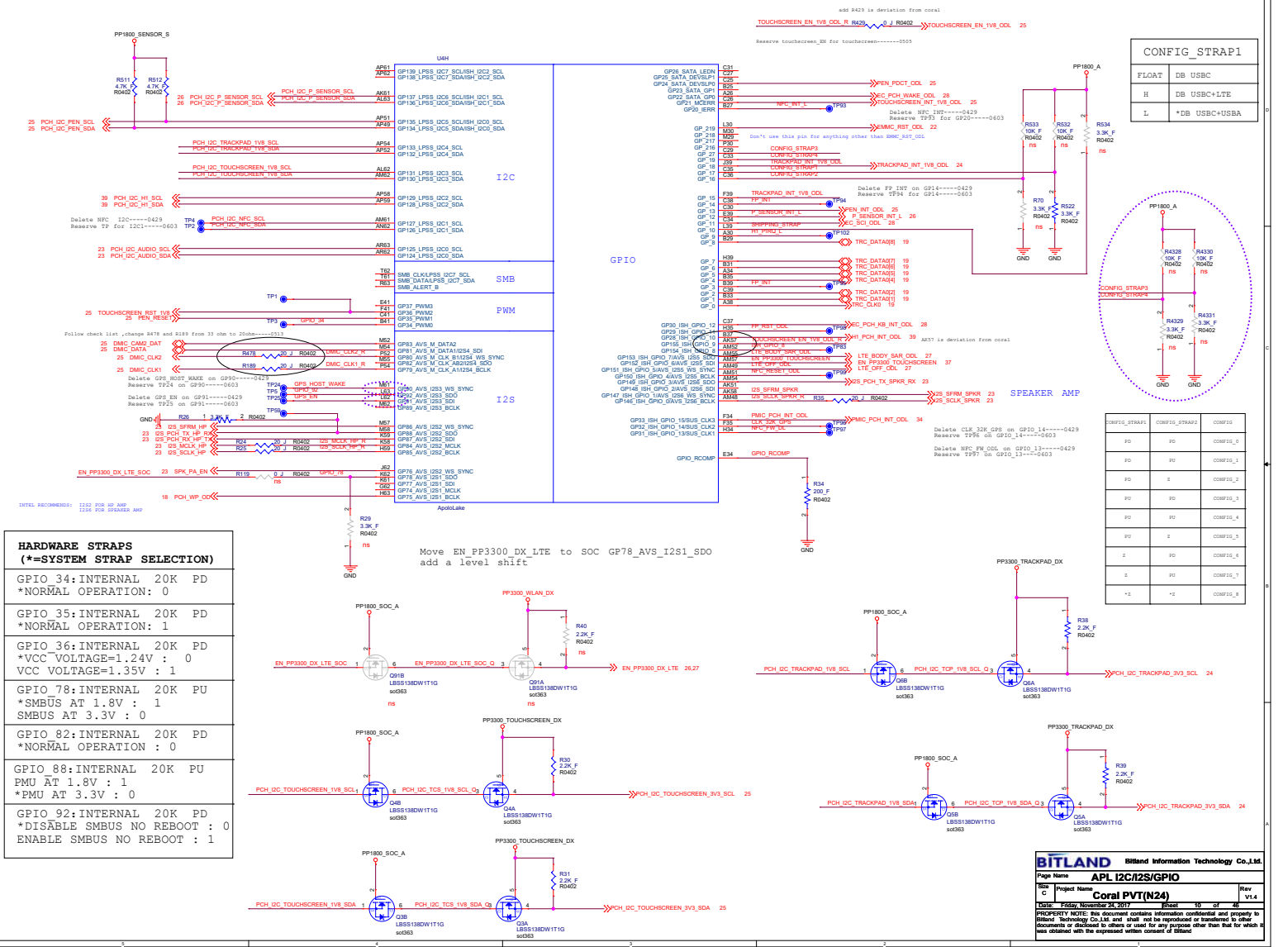
Bus	Alternate function	Schematic net name	Device1	Address1 (7bit)
I2C0	-	PCH_I2C_H1	H1	TBD
I2C1	-	PCH_I2C_NFC (unstuff)	NXP NPC300	0x29 (check 7/8 bit)
I2C2	-	PCH_I2C_AUDIO	HP AMP	0x1A
I2C3	-	PCH_I2C_TOUCHSCREEN	TOUCHSCREEN	TBD
I2C4	-	PCH_I2C_TRACKPAD	TRACKPAD	TBD
I2C5	ISH I2C0	unused		
I2C6	ISH I2C1	unused		
I2C7	ISH I2C2	unused		
SMBUS	I2C7	unused		
PMIC_I2C	-	PCH_I2C_PMIC	PMIC	0x5E

DMIC Diagram





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Page Name		APL PCIE/USB/SATA	
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HARDWARE STRAPS (* = SYSTEM STRAP SELECTION)	
GPIO 34: INTERNAL 20K PD	*NORMAL OPERATION: 0
GPIO 35: INTERNAL 20K PD	*NORMAL OPERATION: 1
GPIO 36: INTERNAL 20K PD	*VCC VOLTAGE=1.24V : 0
VCC VOLTAGE=1.35V : 1	
GPIO 78: INTERNAL 20K PU	*SMBUS AT 1.8V : 1
SMBUS AT 3.3V : 0	
GPIO 82: INTERNAL 20K PD	*NORMAL OPERATION : 0
GPIO 88: INTERNAL 20K PU	PMU AT 1.8V : 1
PMU AT 3.3V : 0	
GPIO 92: INTERNAL 20K PD	*DISABLE SMBUS NO REBOOT : 0
ENABLE SMBUS NO REBOOT : 1	

CONFIG_STRAP1	
Float	DB USBC
H	DB USBC+LTE
L	*DB USBC+USBA

CONFIG1_STRAP1	CONFIG1_STRAP2	CONFIG1_STRAP3
PD	PD	CONFIG12_5
PD	PD	CONFIG12_1
PD	PD	CONFIG12_2
PD	PD	CONFIG12_3
PD	PD	CONFIG12_4
PD	PD	CONFIG12_5
PD	PD	CONFIG12_6
PD	PD	CONFIG12_7
PD	PD	CONFIG12_8

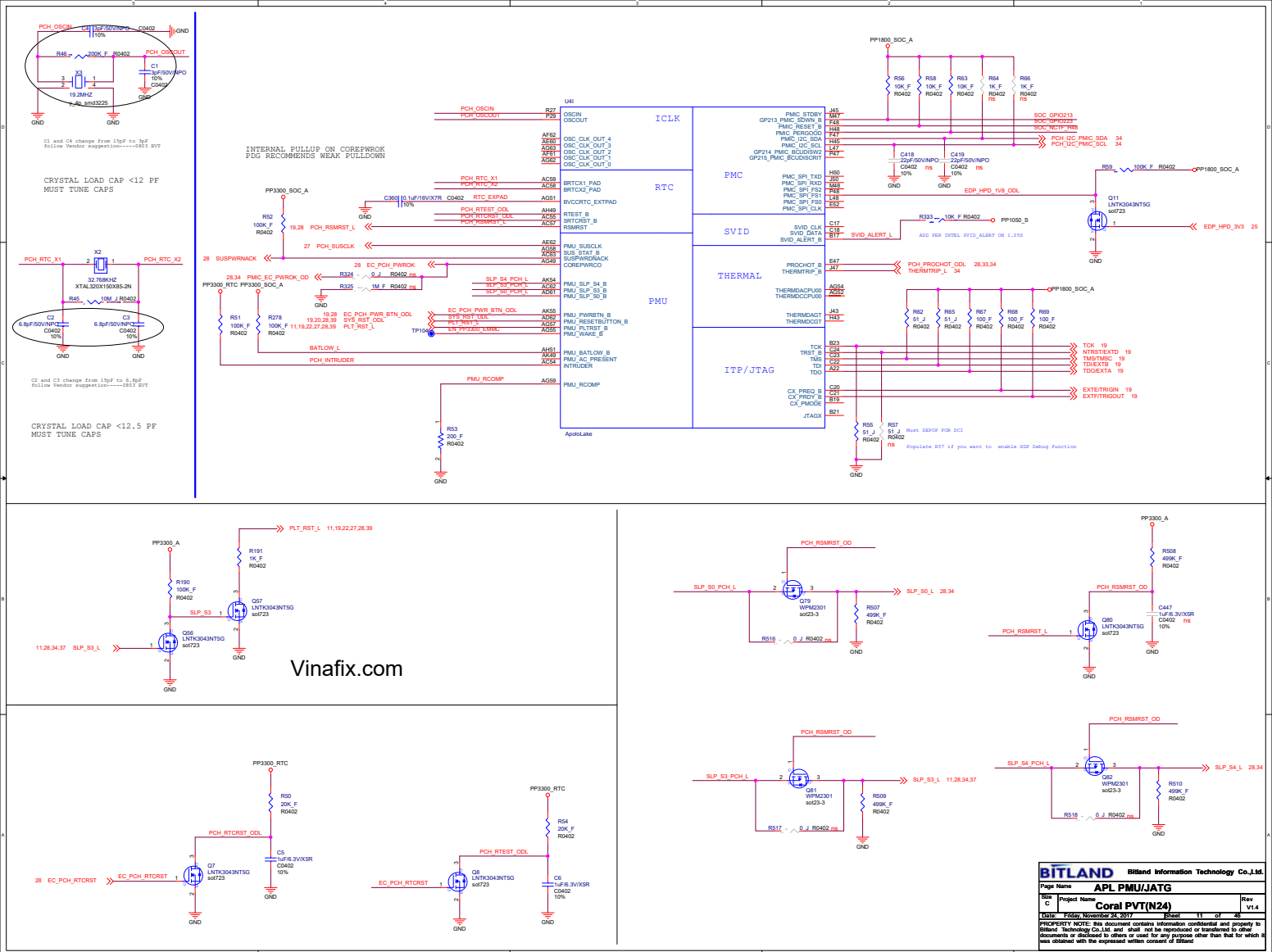
BITLEND Bitland Information Technology Co., Ltd.

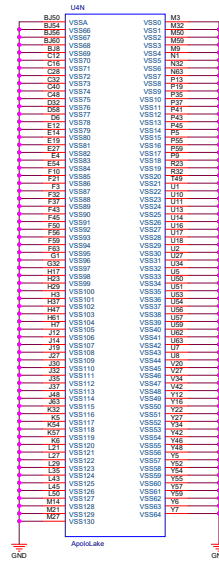
Page Name: **APL I2C/I2S/GPIO**

Doc: **C** Project Name: **Coral PVT(N24)** Rev: **V1.4**

Date: **Friday, November 24, 2017** Sheet: **10** of **24**

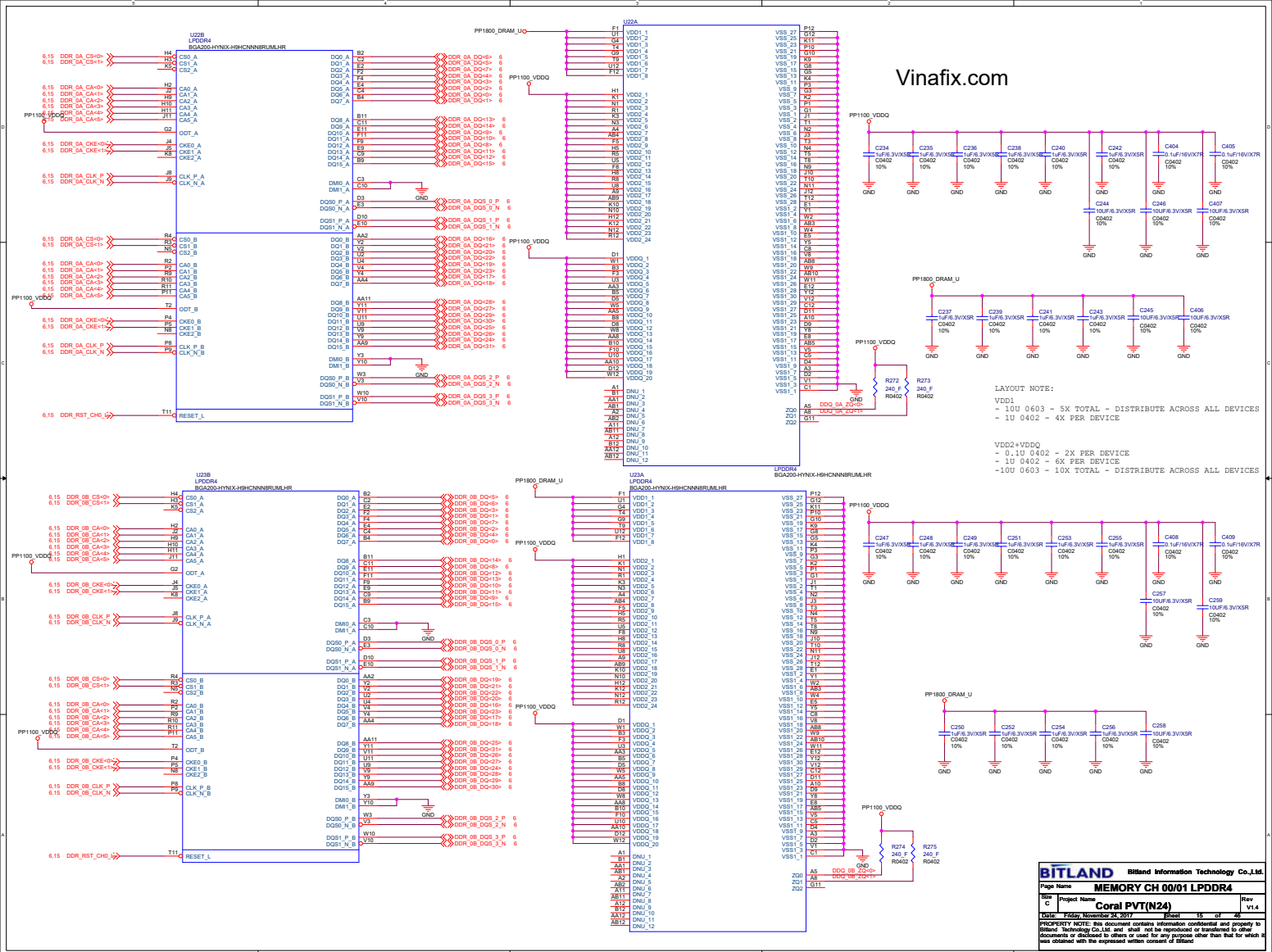
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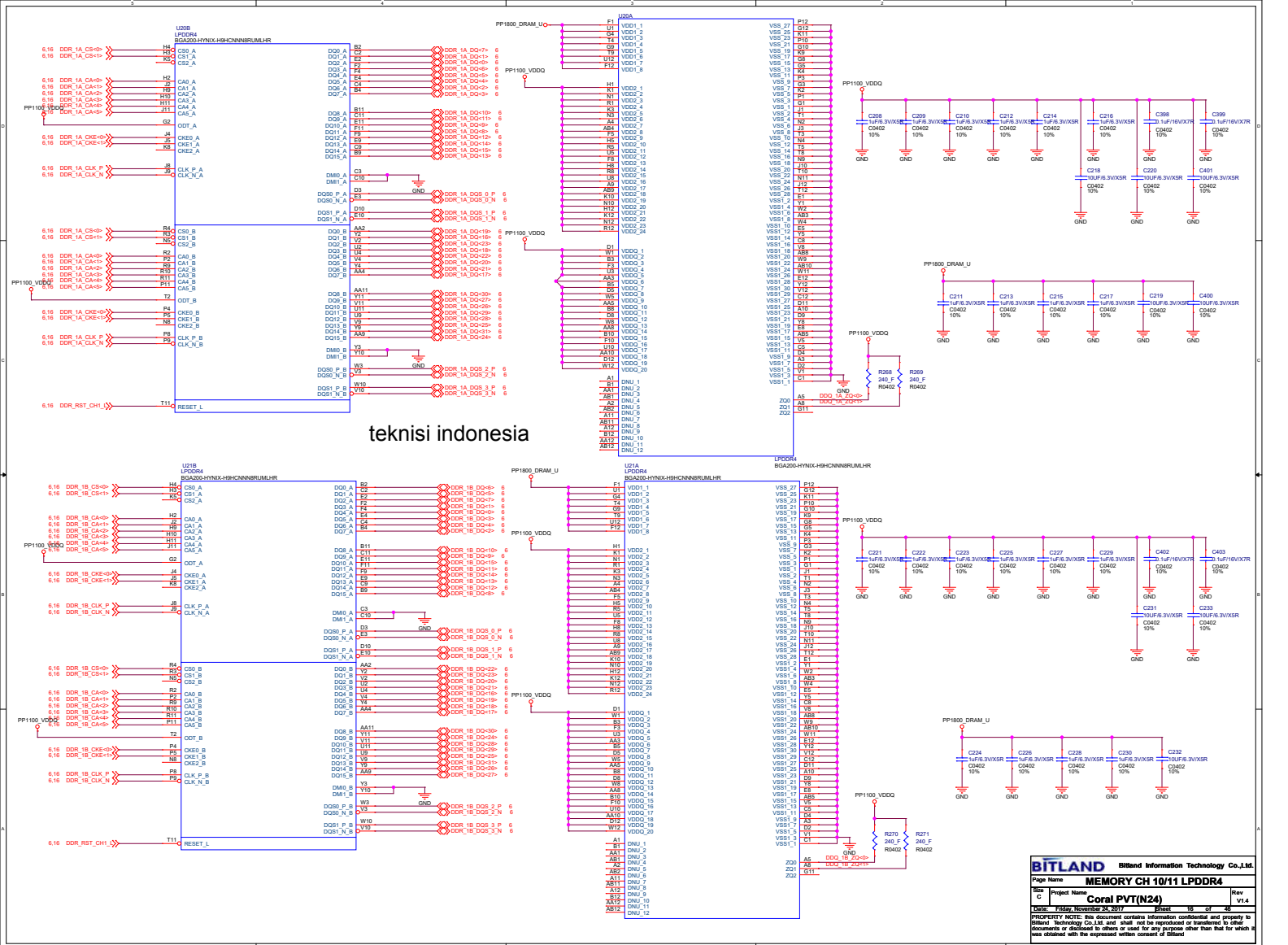


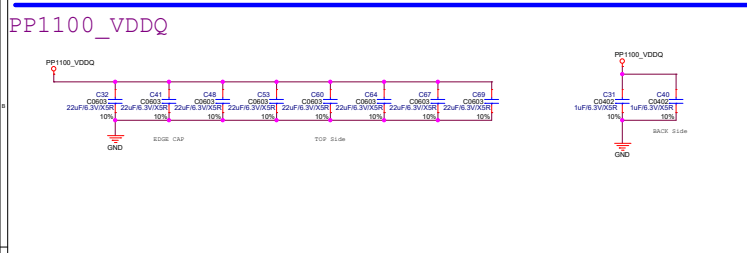
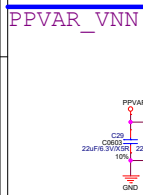


UHO		
L18	MCVR_TDI	MCVR_VCCIN_VRL_RDV H18
E18	MCVR_TDO	
B18	MCVR_TMS	MCVR_PWRGOOD_OUT F18
C18	MCVR_TCK	
D18	MCVR_TRST_B	
B12		MCVR_EXTGREG H12
F12	MCVR_BREAK_B	
T6	MCVR_GP01	A3
C15	MCVR_GP00	MCVR_VT0T_100 G2
	MCVR_VCONPCTL	MCVR_VT0T_100
J18	MCVR_DIGPB0	MCVR_VT0T_58 H10
F15	MCVR_DIGPB1	MCVR_VT0T_58 F9
F14		M12
E6	MCVR_ANAPB0	MCVR_VT0T_548 M10
E6	MCVR_ANAPB1	MCVR_VT0T_24 M10
M18	MCVR_EDM1	MCVR_VT0TVS8 H14
C18	MCVR_EDM0	
F20	MCVR_VCCUSEPRG0	MCVR_ROOMP F12
C9	MCVR_HINCLAREF	
ApollLake		

UHP		
T11	NOCCONNECT10	NOCCONNECT10 F20
L14	NOCCONNECT11	NOCCONNECT11 F20
R18	NOCCONNECT12	NOCCONNECT12 F20
E6	NOCCONNECT13	NOCCONNECT13 F20
R17	MCVR_USBRPT0	NOCCONNECT14 F20
E3	MCVR_USBRPT1	NOCCONNECT15 F20
D1	MCVR_USBRPT2	NOCCONNECT16 F20
A20	MCVR_GP02	NOCCONNECT17 F20
F21	NOCCONNECT18	NOCCONNECT18 F20
B12	NOCCONNECT19	NOCCONNECT19 F20
B01	NOCCONNECT20	NOCCONNECT20 F20
P20	NOCCONNECT21	NOCCONNECT21 F20
A20	SPARE_2	SPARE_2 F20
A20	SPARE_3	SPARE_3 F20
A20	SPARE_4	SPARE_4 F20
ApollLake		







PP1050_VCCRAM_S

PP1050_VCCRAM_S

EDGE CAP

Place near VCCRAM_LF05 FPGAs

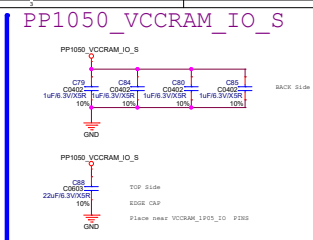
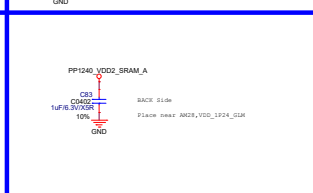


Figure 10 shows two recommended layout diagrams for the PP1240_VDD2_SRAM_A and PP1240_VDD2_IO_A. The left diagram illustrates the SRAM layout, featuring three columns of capacitors (C01, C02, C03) and a top-side capacitor (C04). The right diagram illustrates the IO layout, featuring two columns of capacitors (C05, C06) and a top-side capacitor (C07). Both diagrams include labels for 'BACK Side', 'TOP Side', and 'SIDE CAP'.



PP1240_VDD2_SRAM_A

C76
C77
C76
C77
1uF/8.2V/X5R
1uF/8.2V/X5R
10%
10%
GND

PP1240_VDD2_SRAM_A

C87
C88
22uF/8.2V/X5R
10%
GND

TOP Side
EDGE CAP
Place near A322, A322, A322
VDD2_VDD2_A0D_100_31L

PP1800_SOC_A

C87
C103
C88
1uF/8.2V/X5R
10%
10%
10%
GND

BACK Side
PP1800_SOC_A

C103
C104
1uF/8.2V/X5R
10%
10%
GND

TOP Side
EDGE CAP
Place near VDD1_PRTV_A

Figure 1: Recommended decoupling capacitor placement for the PP3300_SOC_A. The figure contains three circuit diagrams. The first diagram, labeled 'PP1240_VCC02_IO_A', shows a capacitor C18 (0A602) connected between a 1uF/6.3V(X50R) capacitor and the SACK pin of a device, with a note 'Place near A220 VCC02_VP2A_VCC02'. The second diagram, labeled 'PP3300_SOC_A', shows a capacitor C197 (0A602) connected between a 1uF/6.3V(X50R) capacitor and the SACK pin. The third diagram, labeled 'PP3300_SOC_A', shows a more complex decoupling network with capacitors C91 (0A602), C92 (0A602), and C195 (0A602) connected to a 22uF/6.3V(X50R) capacitor and the SACK pin, with a note 'Place near A220 VCC02_VP2A_VCC02'.

PP1240_VDD2_IO_A

C93
C9401
1.65V 10% 10%

C101
C9402
1.65V 10% 10%

C94
C9403
1.65V 10% 10%

BACK S16m

GND

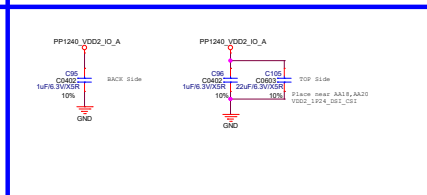
PP1240_VDD2_IO_A

C104
C9601
22µF 10% 10%

TOP S16m

GND

EQ06 CAP
S16m H04F A021,A018,A022,A022
VDD2_VT4_M001



PP3300_RTC

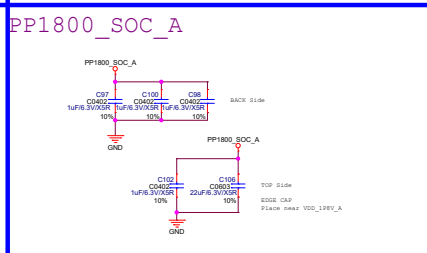
C99
10A0224
1uF/0.5V/50V
10%

C98
0A0022
0.1uF/50V/50V
10%

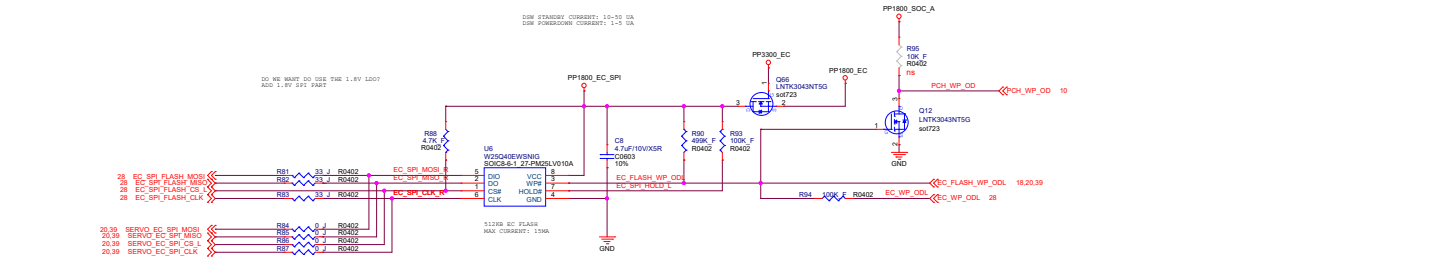
TOP Slide

GND

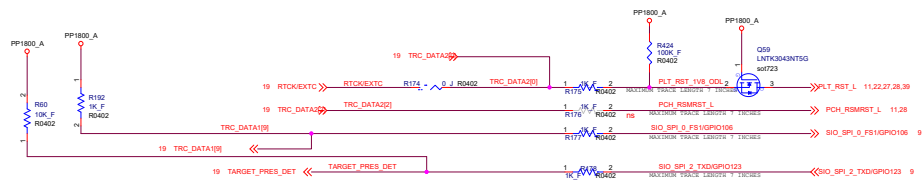
AA14
VCC_RTC_3P3V

[illegible]

EC SPI FLASH



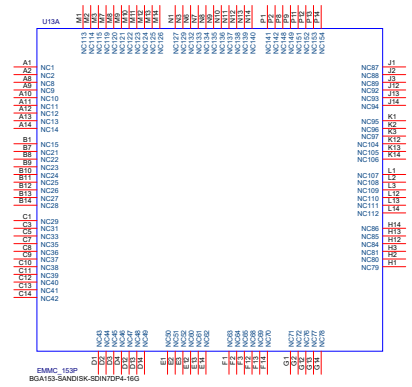
BITLAND		Bittland Information Technology Co.,Ltd.	
Page Name		SPI ROM	
Size	Project Name	Rev	
C	Coral PVT(N24)	V1.4	
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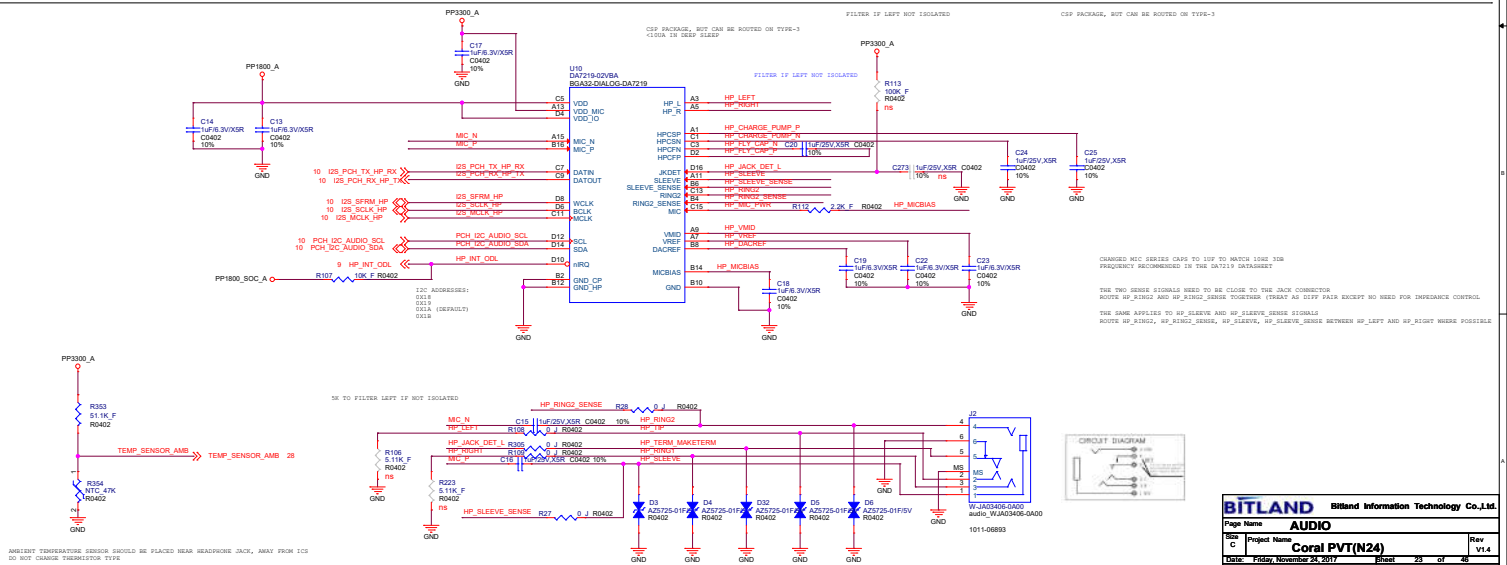
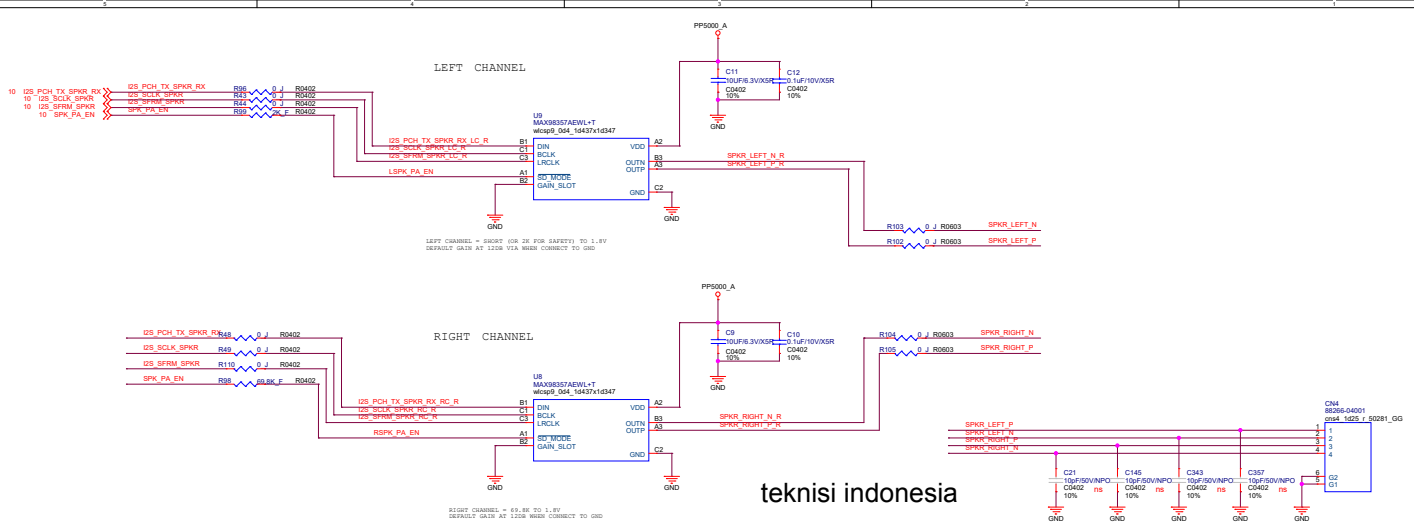
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Page Name			
TPM/SILEGO(Removed)			
Rev	Project Name		Rev
C	Coral PVT(N24)		V1.4
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MICRO SD CARD

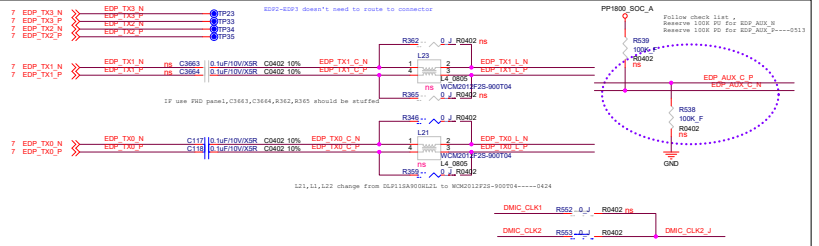


MICRO SD CARD

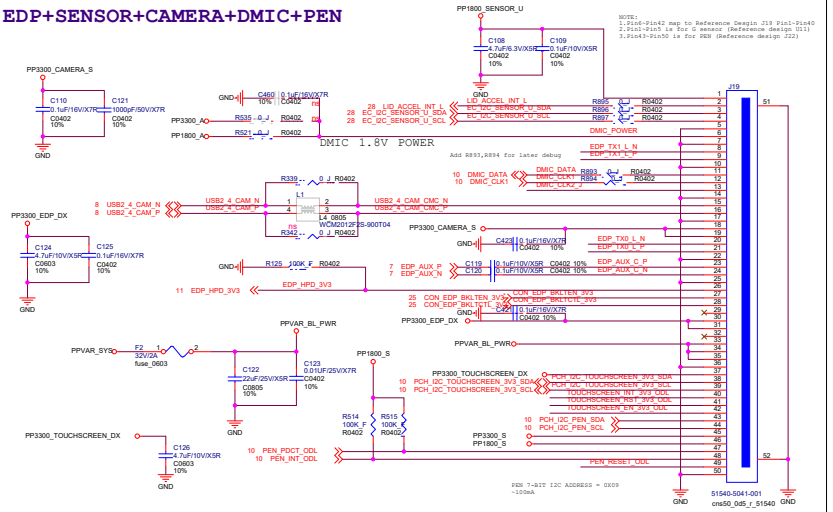
BITLAND		Bitland Information Technology Co.,Ltd.	
Page Name EMMC/SD			
Size C	Project Name Coral PVT(N24)		Rev V1.4
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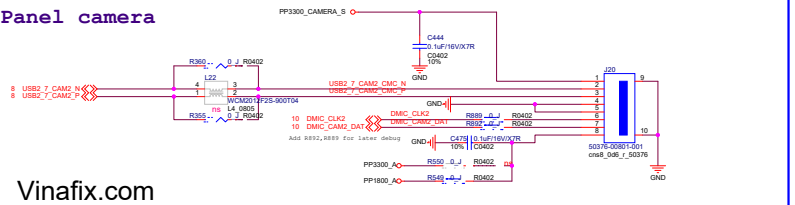
LID ACCEL (MOVE TO PAGE45)



TOUCHSCREEN

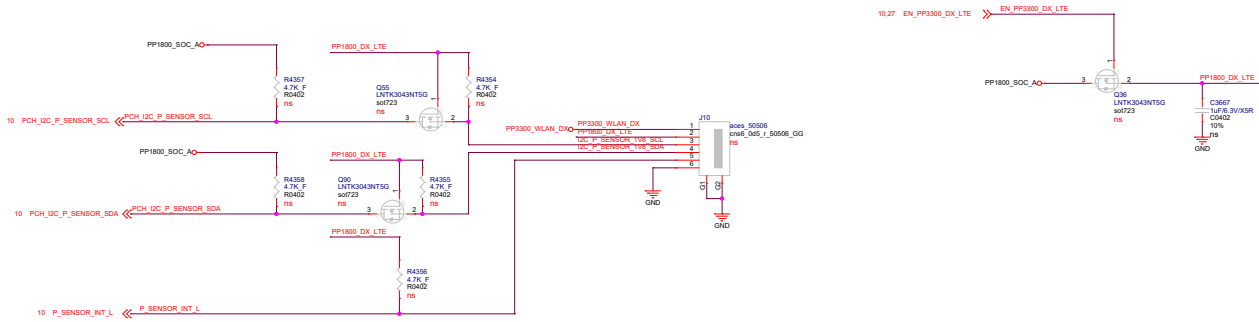


C Panel camera

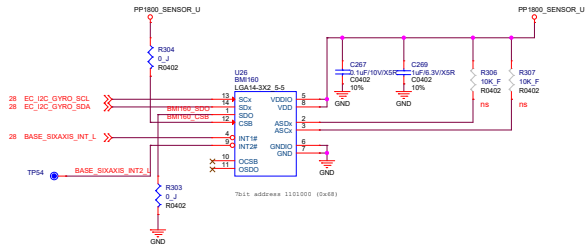


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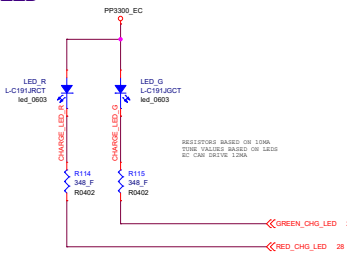
P-SENSOR



GYRO SENSOR

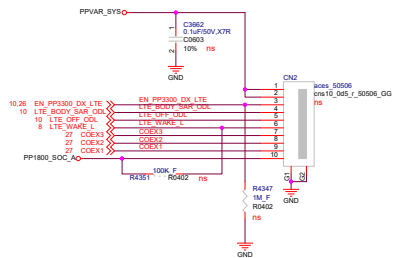


CHARGE/BATTERY LED

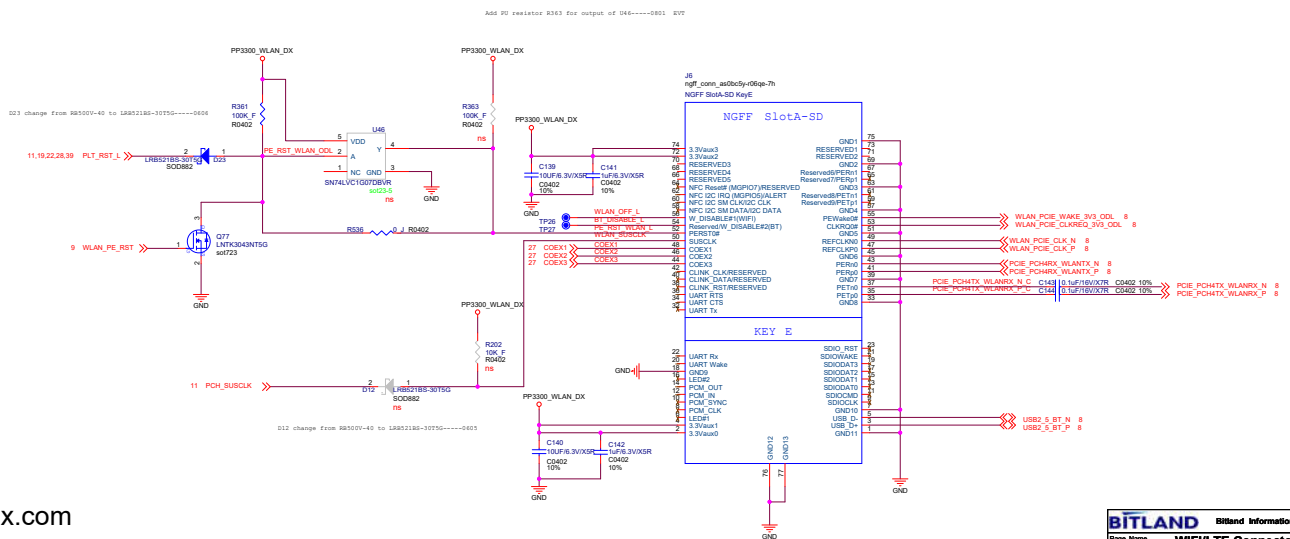


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Page Name		GYRO/CHARGE LED/P-Sensor	
Rev	Project Name		
C	Coral PVT(N24)	Rev V1.4	
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TO LTE/B CONNECTOR



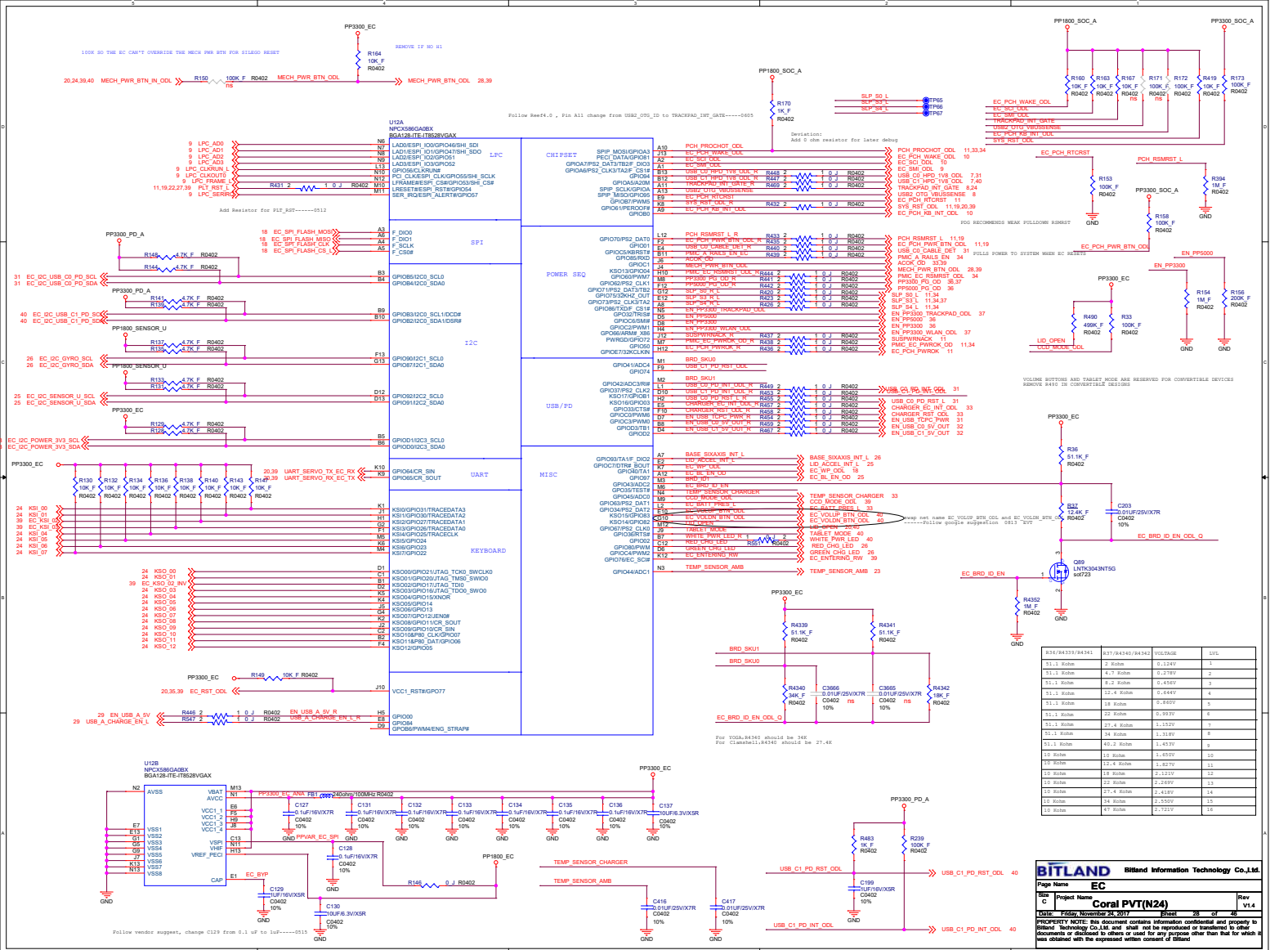
WIFI



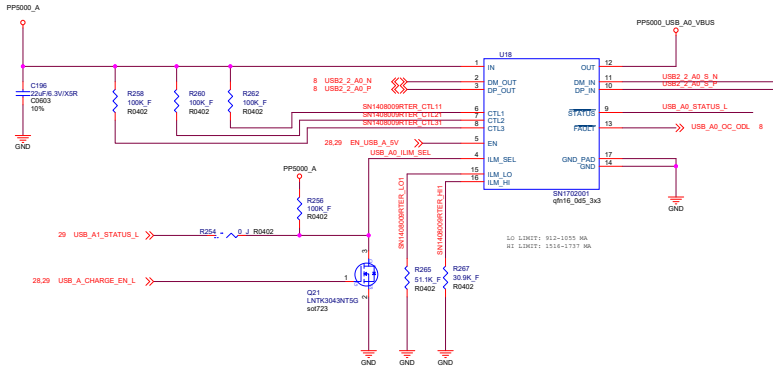
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Page Name WiFi/LTE Connector			
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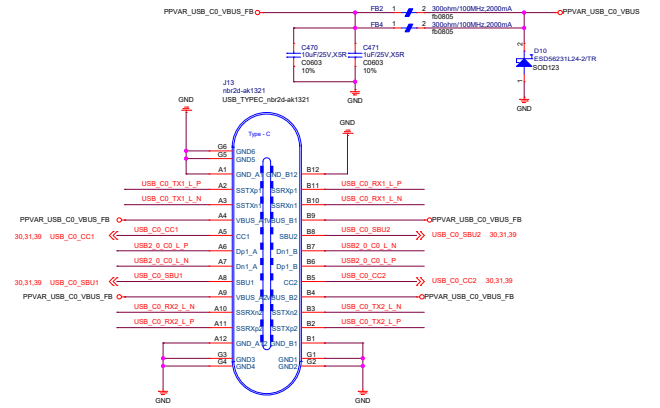
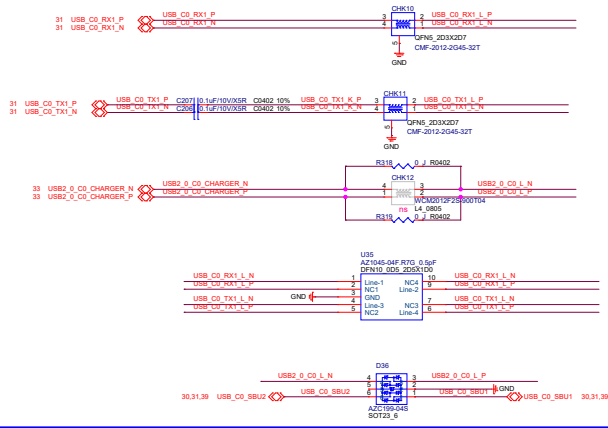
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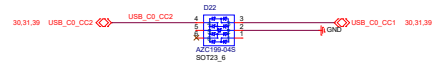
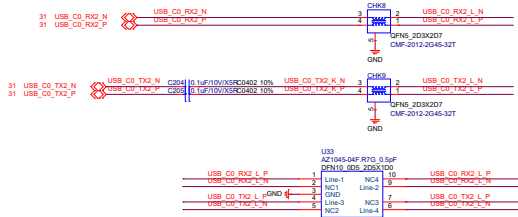
PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR

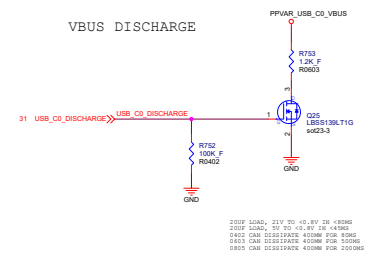


Deviation:
Change L6(PCMF3USB3S) to discrete EMI filter and ESD---0420

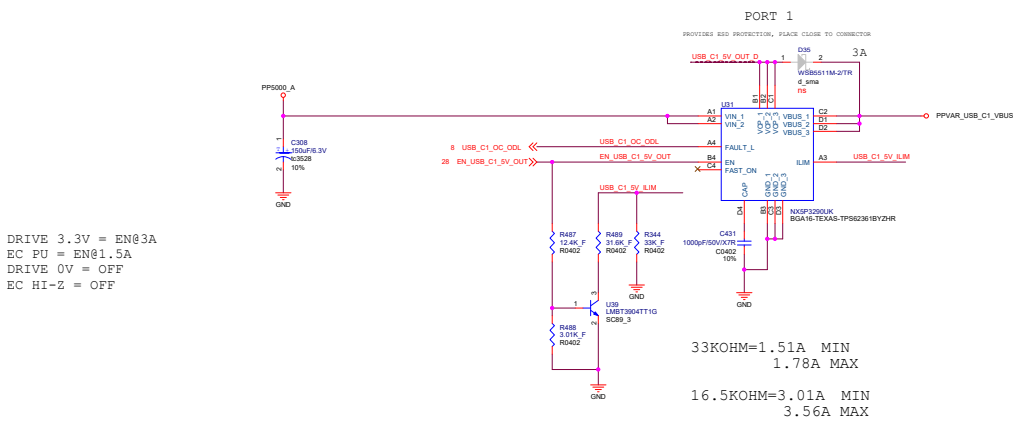


Deviation:
Change L7(PCMF3USB3S) to discrete EMI filter and ESD---0420

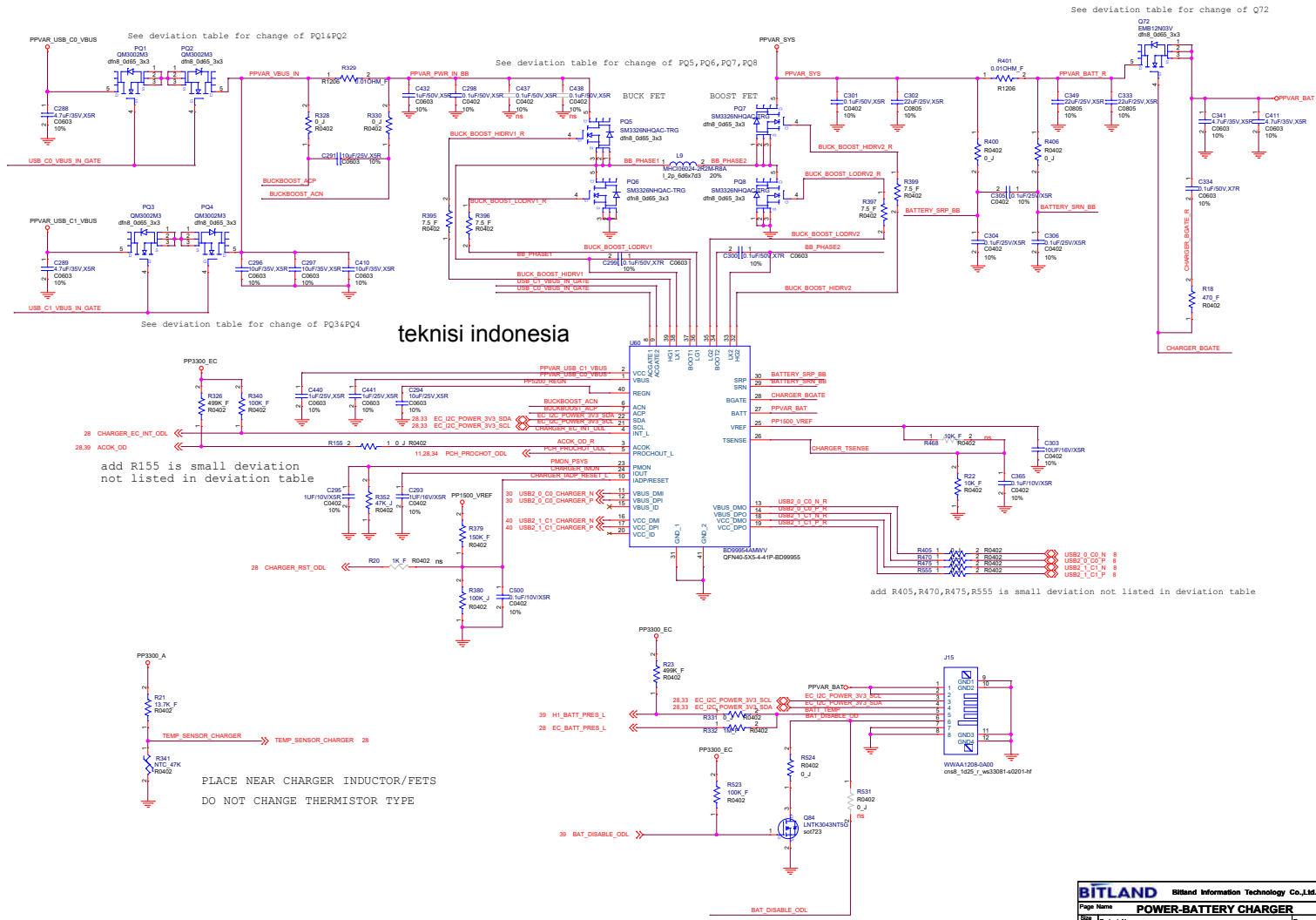




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Page Name USB C 5V OUT			
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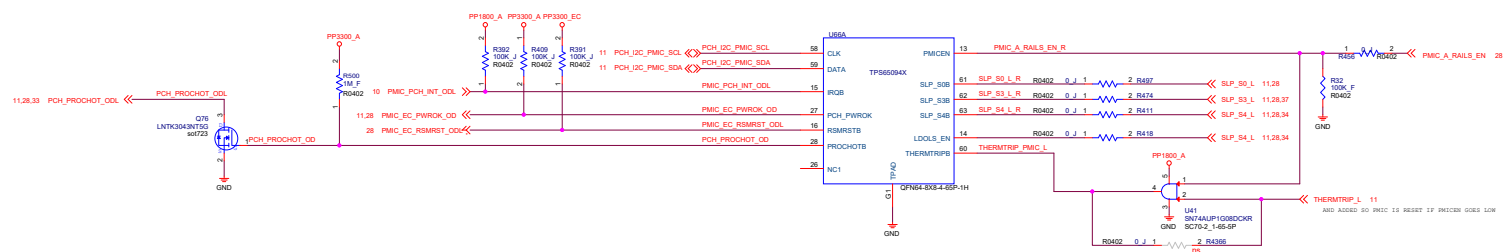
tekni indonesia

add R155 is small deviation
not listed in deviation table

add R405,R470,R475,R555 is small deviation not listed in deviation table

PLACE NEAR CHARGER INDUCTOR/FETS
DO NOT CHANGE THERMISTOR TYPE

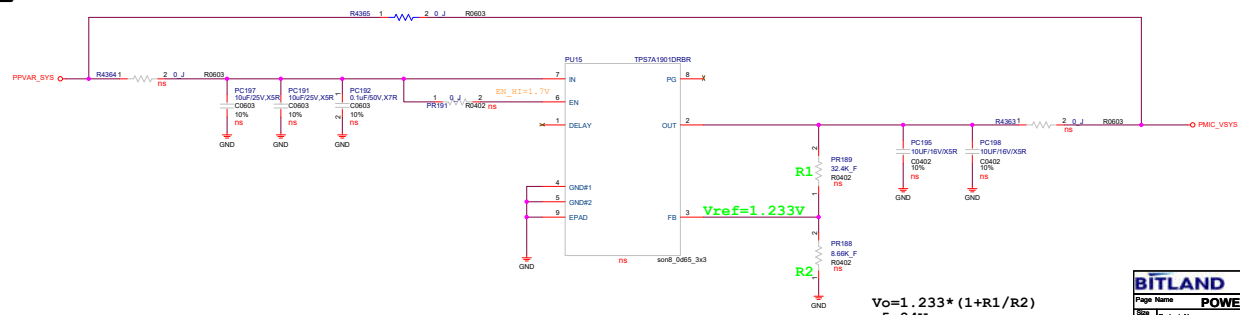
BITLAND			
Bitland Information Technology Co., Ltd.			
Page Name	POWER-BATTERY CHARGER		
Rev	1	Rev	1.4
Date	2021-11-24	Sheet	1 of 1
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adding R497/R474/R411/R418 is small deviation from Coral for later debug

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PMIC_VSYS



$$V_o = 1.233 \times (1 + R1/R2)$$

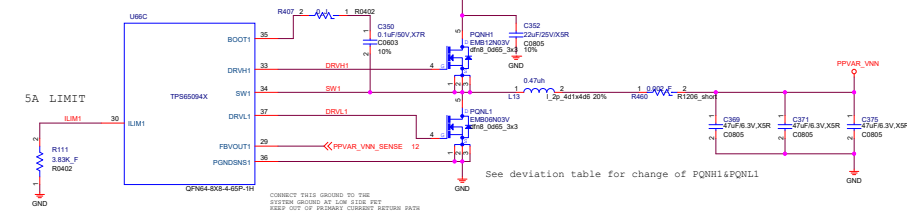
$$= 5.84V$$

$$\text{Note: } (R1 + R2) = 10K - 100K$$

BITLAND			
Bitland Information Technology Co., Ltd.			
Page Name	POWER-PMIC LOGIC		
Rev	1.0	Project Name	Coral PVT(N24)
Date	2024-10-28	Sheet	14 of 48
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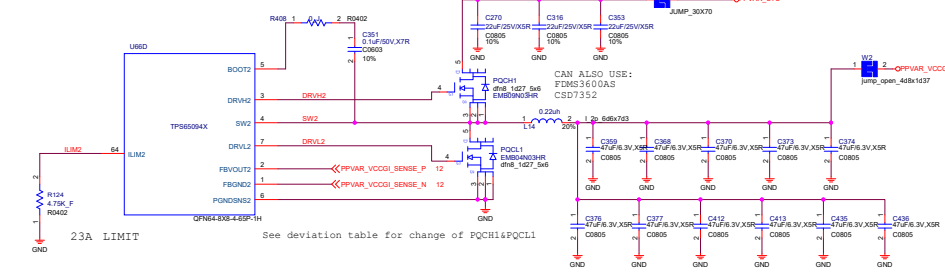
PPVAR_VNN

IPEAK = 3.3A, ITDC = 1.5A



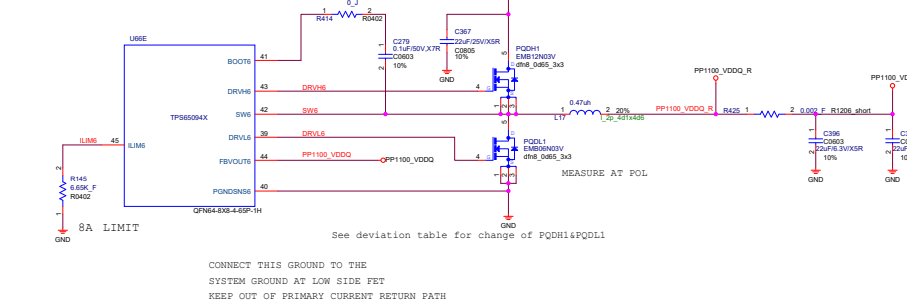
PPVAR_VCCGI

IPEAK = 21A, ITDC = 18A



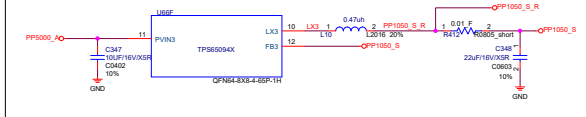
PP1100_VDDQ

IPEAK = 6.74A



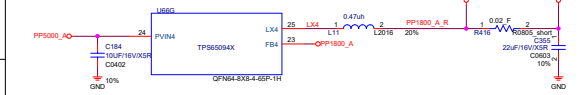
PP1050_S

IPEAK = 2.7A



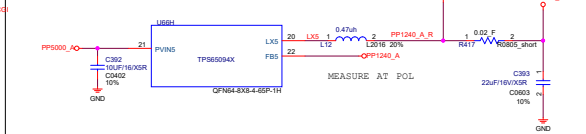
PP1800_A

IPEAK = 1.3A



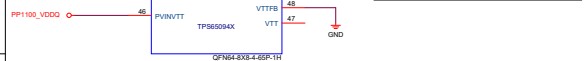
PP1240_A

IPEAK = 1.93A

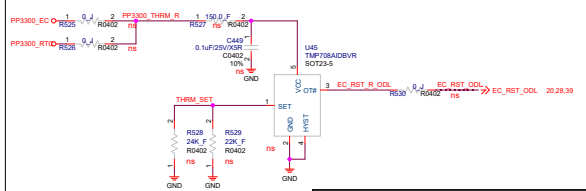


PP0550_VTT

RESISTOR NOTE:
R421, R422, R425 CAN BE .005 OHMS

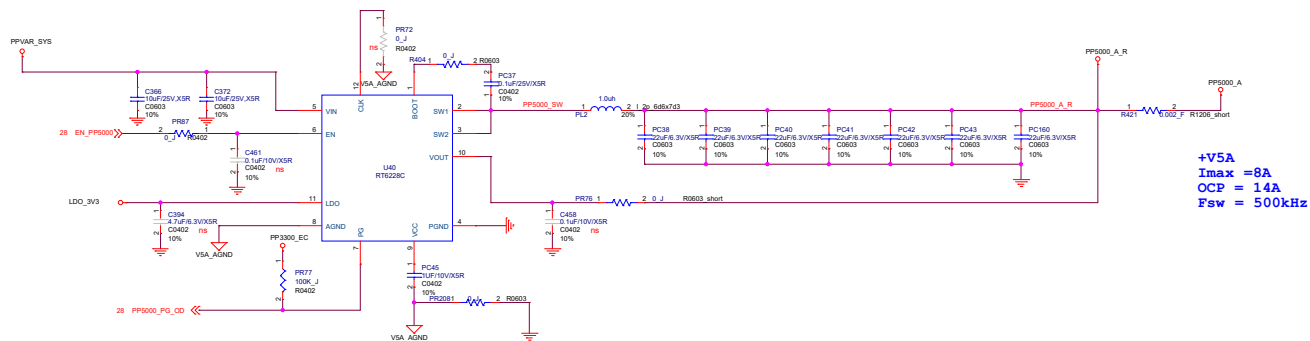
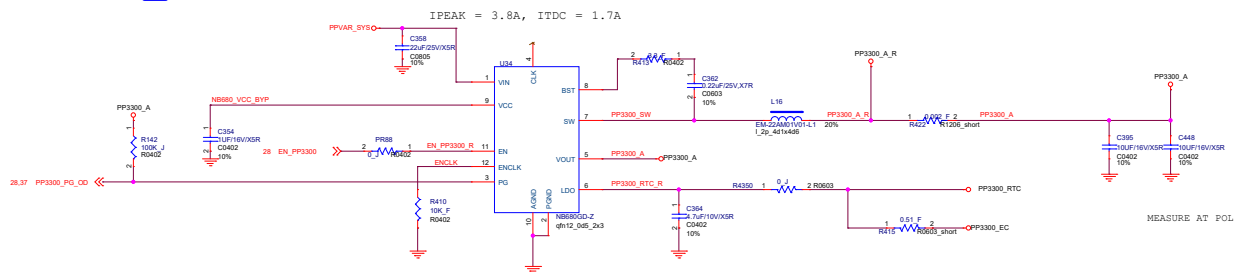


PER TI CAN BE DISCONNECTED IF VTT IS DISABLED

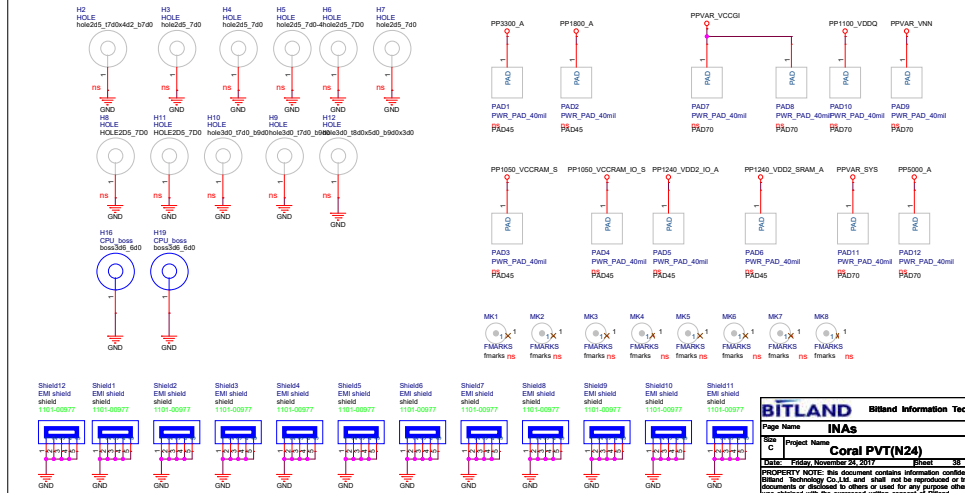
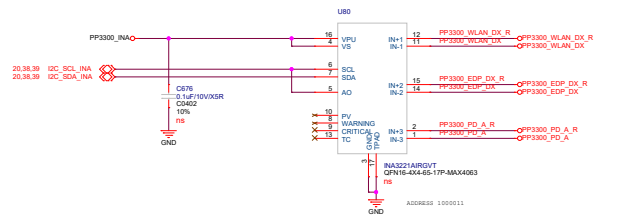
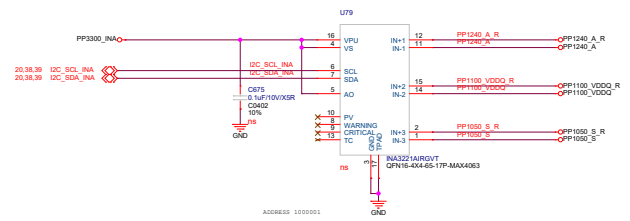


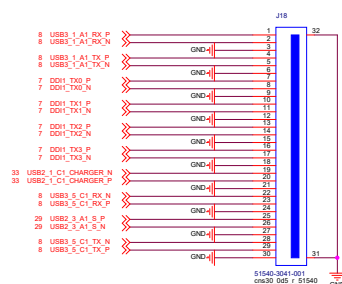
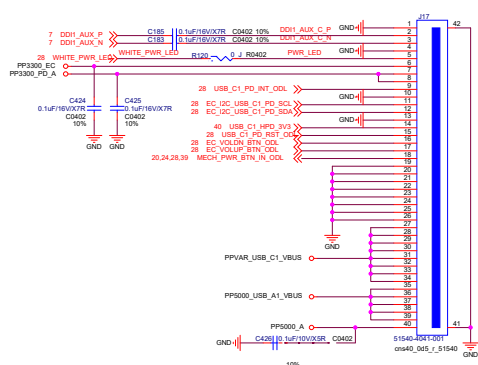
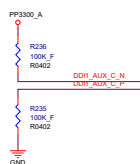
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Page Name	POWER-PMIC RAILS		
Rev	C	Project Name	Coral PVT(N24)
Rev		Rev	V1.4
<p>DATE: 2024-09-28 2024</p> <p>PROPERTY NOTE: This document contains information confidential and property of Bitland Technology Co., Ltd. and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained with the expressed written consent of Bitland</p>			

PP5000_A

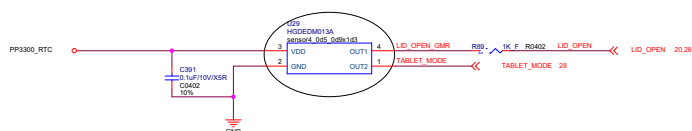
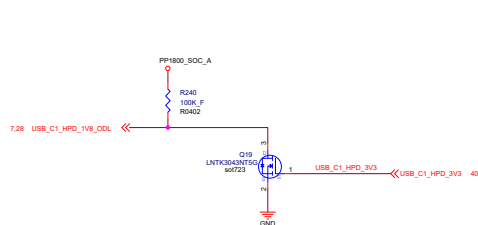


this deviation, please See deviation in deviation list table





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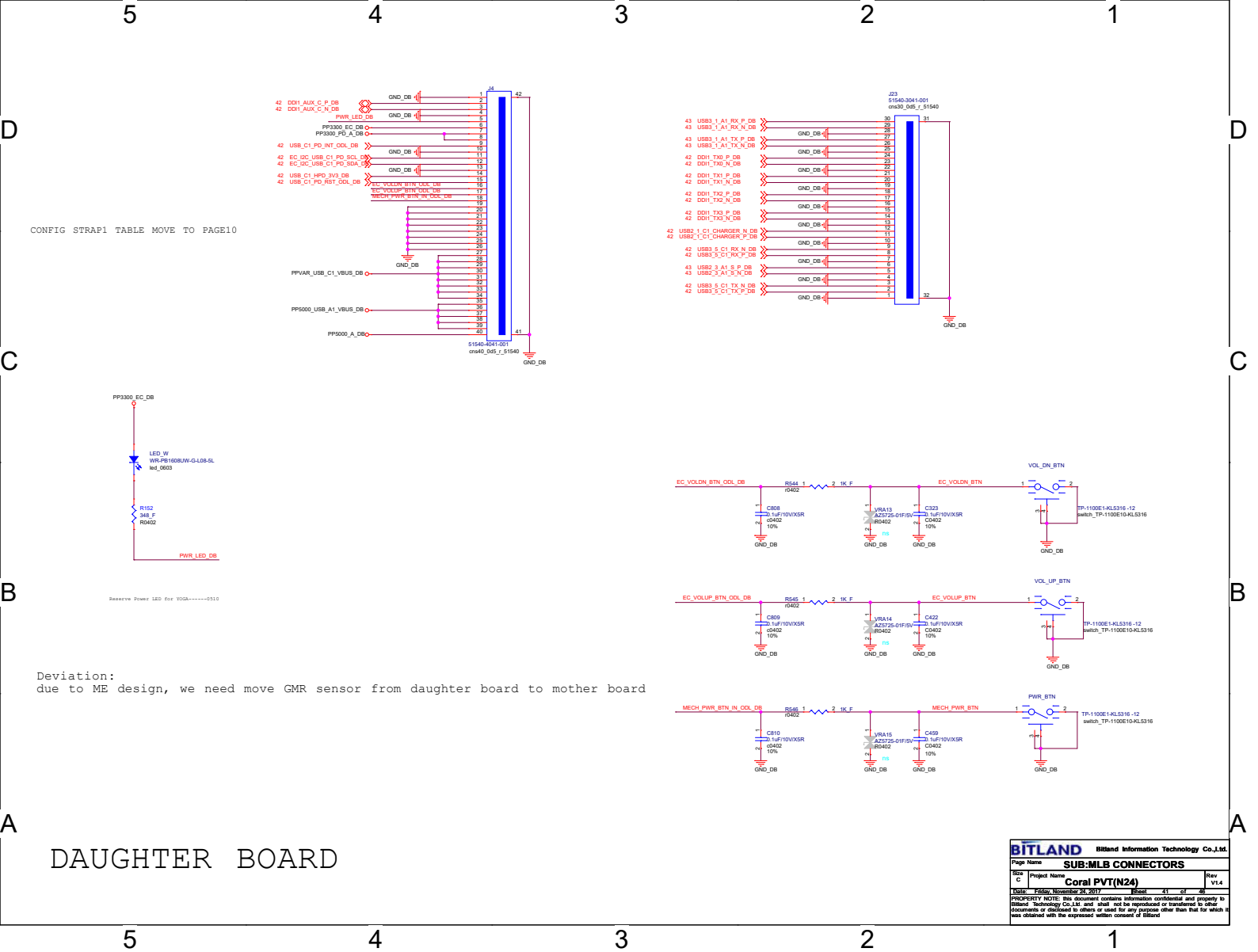


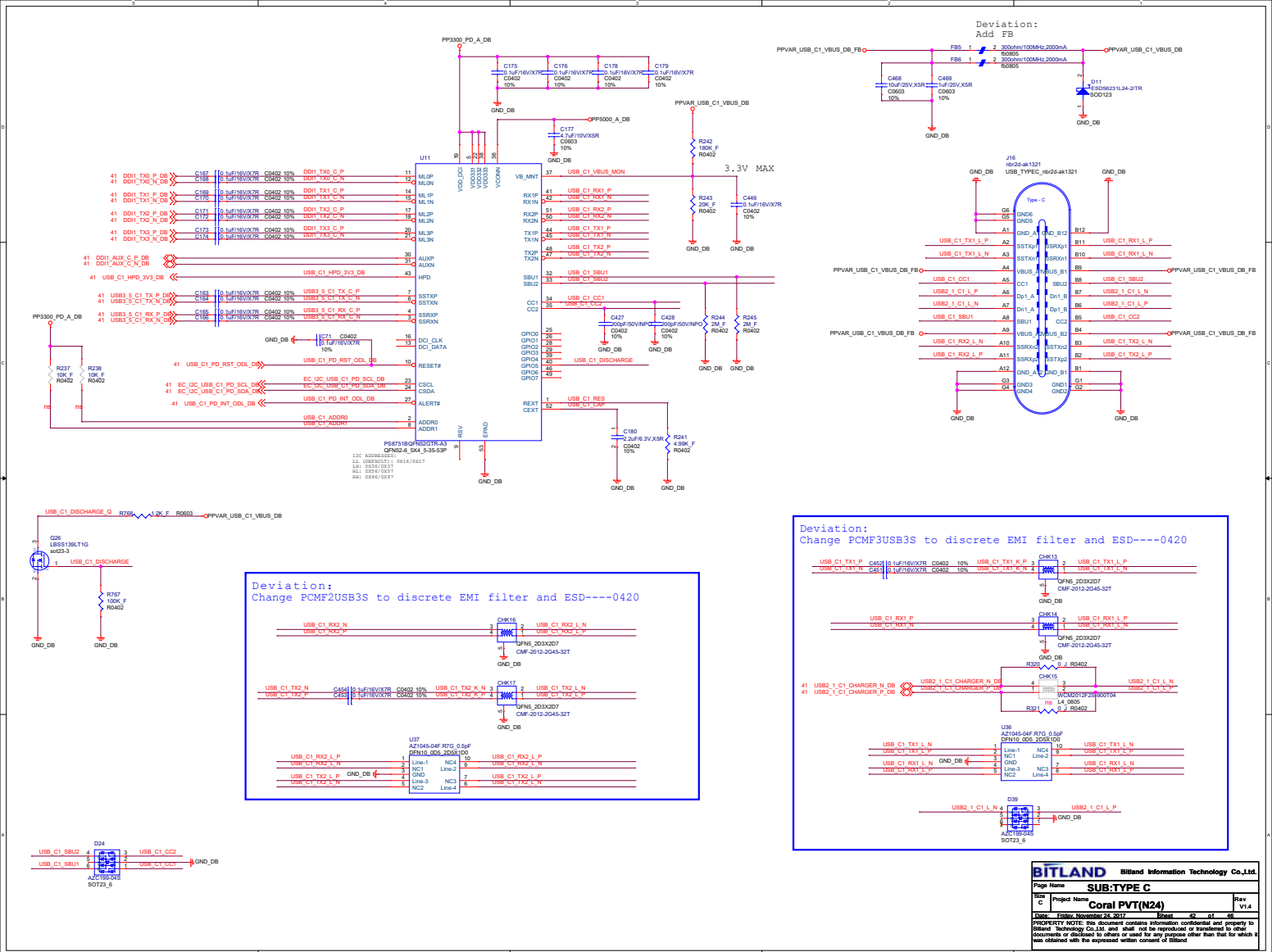
Deviation:
due to ME design, we need move GMR sensor from daughter board to mother board

MOTHER BOARD

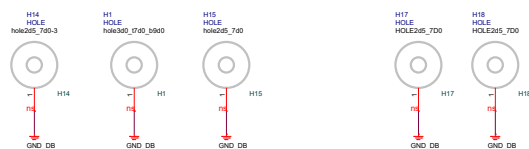
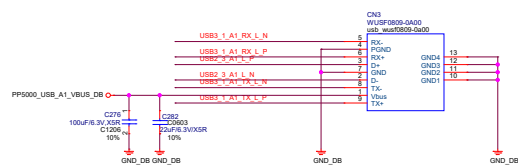
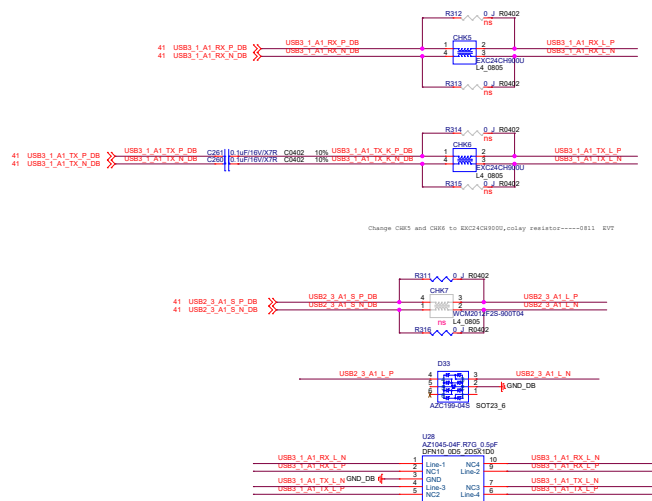
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Page Name		MLB CONNECTORS	
Size C	Project Name	Rev	
	Coral PVT(N24)	V1.4	
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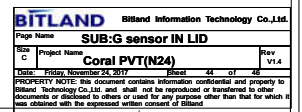
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Deviation:
Change L18(PCMF3USB3S) to discrete EMI filter and ESD---0420





Components that should be DNS to remove feature

Barometer	NFC	GPS	Finger Print	INA (MP Only)	MIPi60	Silego	TPM (not yet approved for DNS)
U1	J11	J14	J10	R741	everything on MIPi60 Debug Header page	U24	D31
R457	C191	C677	C185	R742		C262	Q23
C266	C193	C662	C186	C673		R300	R294
C268	C187	R317	R42	U77	Servo (MP Only)	Q24	R299
R302	C188			U79			U25
Q15	C189			C675	everything on Servo page		C263
R122	C194			U80			C264
Q14	R251			C676			C265
R121	R40			U78			
	Q41			C674			
	R388			C280			
	C323			R159			
	R374			Q17			
	Q38			C281			
	R19			R161			
	R179			C442			
				Q75			
				C443			

NOTE:Barometer/NFC/GPS/Fingerprint/Silego/TPM are all removed

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SCHEMATIC CHANGES

[illegible]

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